LT7688

High Performance TFT Panel Controller of Uart Interface

◆ Introduction

LT7688 is a high-efficient graphic acceleration display controller. It integrated Levetop's 32Bit MCU - LT32U02 and the core structure of TFT Graphic Accelerator - LT7680. Its main function is to provide UART, USB communication, enable system's MUC to send TFT screen displaying content to TFT driver via simple command. The chip support graphic acceleration, PIP, Geometric Drawing, and promote TFT display efficiency, and reduce the upper MCU processing time on graphic, it support 16/18bits RGB type TFT Panel from 320*240(QVGA) to 1280*1024 (SVGA).

The maximum of main frequency of LT7688 internal MCU is 72MHz, includes 64Kbytes Flash and 8Kbytes SRAM. Beside provides UART and USB serial communication, it also provides some analog input AIN, PWM and INT interrupt interfaces. These interfaces can also be set as general purpose IO interfaces. In order to achieve multi-layer, high resolution display effect, LT7688 has 128Mb built-in display memory to support 1bit/pixel to 18bit(262K)/pixel color display. It also owns built-in geometric drawing engine to support point drawing, line drawing, curve drawing, ellipse, triangle, rectangle, rounded rectangle drawing and so on. In addition, the chip has embedded hardware graphics processing unit to provide mandatory graphical operations like magic rotation, flip, reflect, PIP(picture in picture) , hybrid graphics and transparent display. If work with Levetop's TFT module develop software will have better efficiency, and no need to upgrade MCU for TFT screen. The powerful performance of LT7688 is suitable for embedded systems with TFT-LCD display, such as home appliances, industrial control, electronic instruments, medical equipment, human-machine interface, industrial equipment, testing equipment, etc.
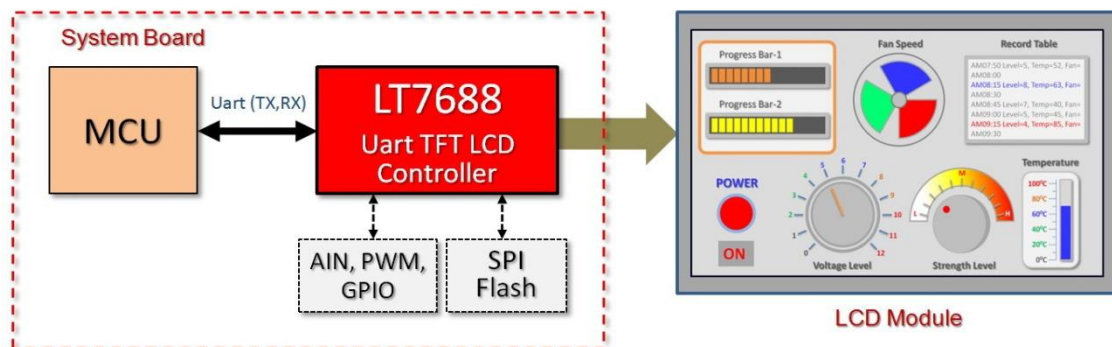
◆ Application Diagram

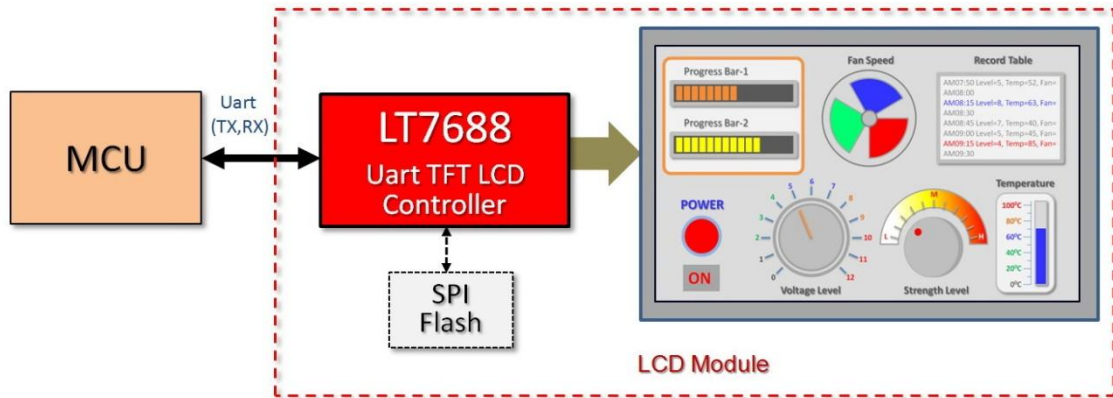**Figure 1：LT7688 Designed on the System Board**

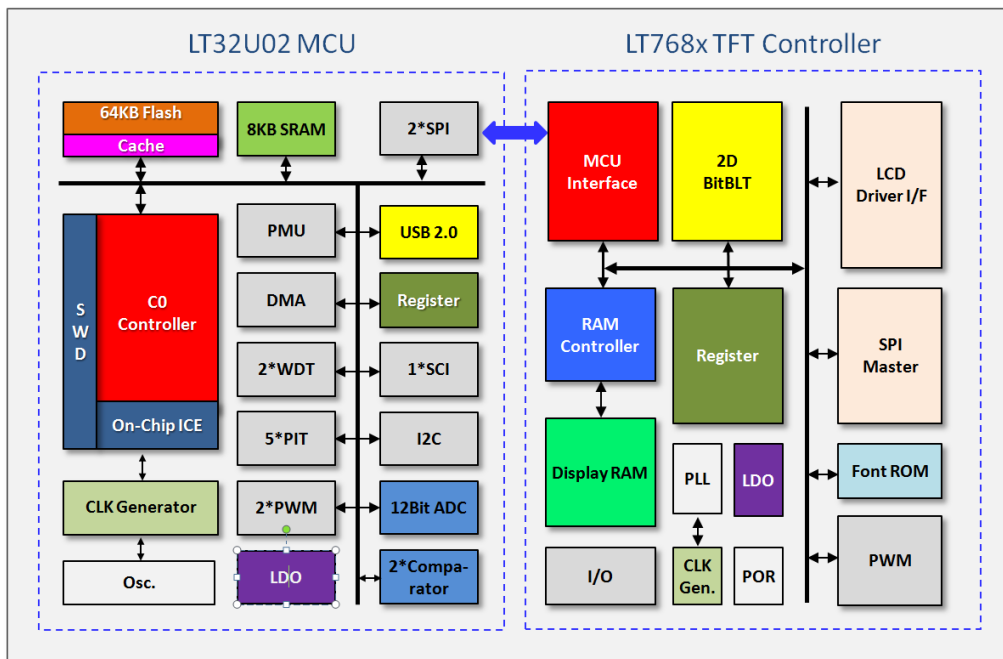**Figure 2: LT7688 Designed on the TFT Module**

Internal Block Diagram

Figure 3: LT7688 Block Diagram

Product Type

Table 1: Product Type

Model Name	Package	Embedded Display RAM	Resolution (Max.)	Color
LT7688	QFN-80 (9*9)	128Mb	1280*1024	262K Color

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⬥ Features

System MCU Interface
- Support SCI/Uart and USB Interface.
- Embedd 32Bit MCU with 72MHz Clock.

USB Interface
- Supports USB2.0 Full Speed.

SCI (Uart) Interface
- Suooprt SCI (Serial Communications Interface).

Memory
- MCU Embedded 64K bytes Flash.
- MCU Embedded 8K bytes SRAM.
- TFTController Embedded 128Mb Display RAM.

Display Data Formats
- 1bpp: Monochrome Data (1-bit/Pixel)
- 8bpp: RGB 3:3:2 (1-byte/Pixel)
- 16bpp: RGB 5:6:5 (2-byte/Pixel)
- 18bpp: RGB 6:6:6 (3bytes/Pixel).
  - ➢ Index 2:6 (64 Index Colors/Pixel with Opacity Attribute)
  - ➢ αRGB 4:4:4:4 (4096 Colors/Pixel with Opacity Attribute)

Support Panel and Resolution
- 支援 16、18bits RGB 介面面板.
- Supported Resolution:
  - ➢ QVGA   : 320*240, 16/18-bit LCD Panel
  - ➢ WQVGA : 480*272, 16/18-bit LCD Panel
  - ➢ VGA   : 640*480, 16/18-bit LCD Panel
  - ➢ WVGA   : 800*480, 16/18-bit LCD Panel
  - ➢ SVGA   : 800*600, 16/18-bit LCD Panel
  - ➢ WSVGA : 1024*600, 16/18-bit LCD Panel
  - ➢ XGA   : 1024*768, 16/18-bit LCD Panel
  - ➢ SXGA   : 1280*1024, 16/18-bit LCD Panel

Display Functions
- Multiple Display Buffer: Multi buffering allows the main display window to be switched among buffers. Multi buffering allows a simple animation display to be performed by switching the buffers
- Horizontal/Vertical Flip Display: Vertical Flip display functions are available for image data reads. PIP window will be disabled if flip display function enable
- Mirror and Rotation Functions are Available for Image Data Writes

- Provide four User-defined 32*32 Pixels Graphic Cursor
- Virtual Display: Virtual display is available to show an image which is larger than LCD panel size. The image may scroll easily in any direction
- Picture-in-Picture (PIP) Display: Supported two PIP windows area: Enabled PIP windows are always displayed on top of Main window. The PIP1 window is always on top of PIP2 window
- Wake-up Display: Wake-up Display is available to show the display data quickly which data is stored in Display RAM. This feature is used when returning from the Standby mode or Suspend mode
- Initial Display: Embedded a tiny processor with 12 instructions and use to show display data which stored in the serial flash and need not external MPU participate. It will auto execute after power-on, until program execute complete then handover control rights to external MCU
- Color Bar: It could display color bar on panel directly. Default resolution is 640 dots by 480 dots.

Bit Block Transfer Engine (BitBLT)
- 2D BTE Engine
- Copy Image with Raster Operators
- Color Depth Conversion
- Solid Fill & Pattern Fill
- Provide User-defined Patterns with 8*8 Pixels or 16*16 Pixels
- Opacity (Alpha-Blend) Control: It blends two images and then generates a new image
  - ➢ Chroma-Keying Function: Mixes images with applying the specified RGB color according to transparency rate
  - ➢ Window Alpha-Blending Function: Mixes two images according to transparency rate in the specified region (fade-in and fade-out functions are available)
  - ➢ Dot Alpha-Blending Function: Mixes images according to transparency rate when the target is a graphics image in the RGB format.

Shape Drawing Engine
- Provide Smart Drawing Features: Line, Rectangle, Triangle, Polygon, Poly-Line, Circle, Ellipse, Arc, Rounded-Rectangle and Circle-Rectangle

Text Features

- Embedded 8*16, 12*24, 16*32 Character Sets of ISO/IEC 8859-1/2/4/5.
- User-defined Characters Support Half Size & Full Size for 8*16, 12*24 and 16*32.
- Programmable Text Cursor for Writing with Character.
- Character Enlargement Function *1, *2, *3, *4 for Horizontal/Vertical Direction.
- Support Character Rotates 90 Degree.

SPI Master Interface

- Provide DMA Function: Support Direct Data Transfer from External Serial Flash to Frame Buffer
- Compatible with Standard SPI Specifications
- Provides 16bytes Read FIFO and 16bytes Write FIFO
- Provide Interrupt when Tx FIFO was Empty and SPI Tx/Rx Engine Idle.

I2C Interface

- MCU Provide I2C Interface.
- Support Standard Mode (100kbps) and Fast Mode (400kbps).

PWM Interface

- MCU Provide 4 PWM Output.
- TFT Controller Embedded Two 16bits Counter and 2 PWM Output.
- Programmable Duty Control of Output Waveform (PWM).

Interrupt Signals

- MCU Provide 6 Interrupt Inputs.
- TFT Controller Provides 1 Interrupt Output.

GPIO

- MCU Supports 10 GPIO.
- TFT Controller Provides 8 GPIO.

Analog Input

- MCU Provide 2 ADC's Analog Input.
- Embedded Comparator

Reset

- MCU Provides Power-On-Reset, External Reset, Software Reset, WatchDog Reset and Voltage Detect Reset
- TFT Controller Power-On-Reset, External Reset, Software Reset.

Power Saving Mode

- Provide Standby, Suspend and Sleep Mode.
- Support MCU Wakeup.

Clock Source

- MCU Embedded a Clock upto 72MHz.
- Support 32.768Khz External Crystal Oscillator Circuit.
- Embedded Programmable PLL for Core Clock, LCD Panel's Pixel Clock and Frame Buffer Clock.

Power Supply

- VDD Power: 3.3V +/- 0.3V.
- Embedded 1.5V、1.8V LDO.

Package

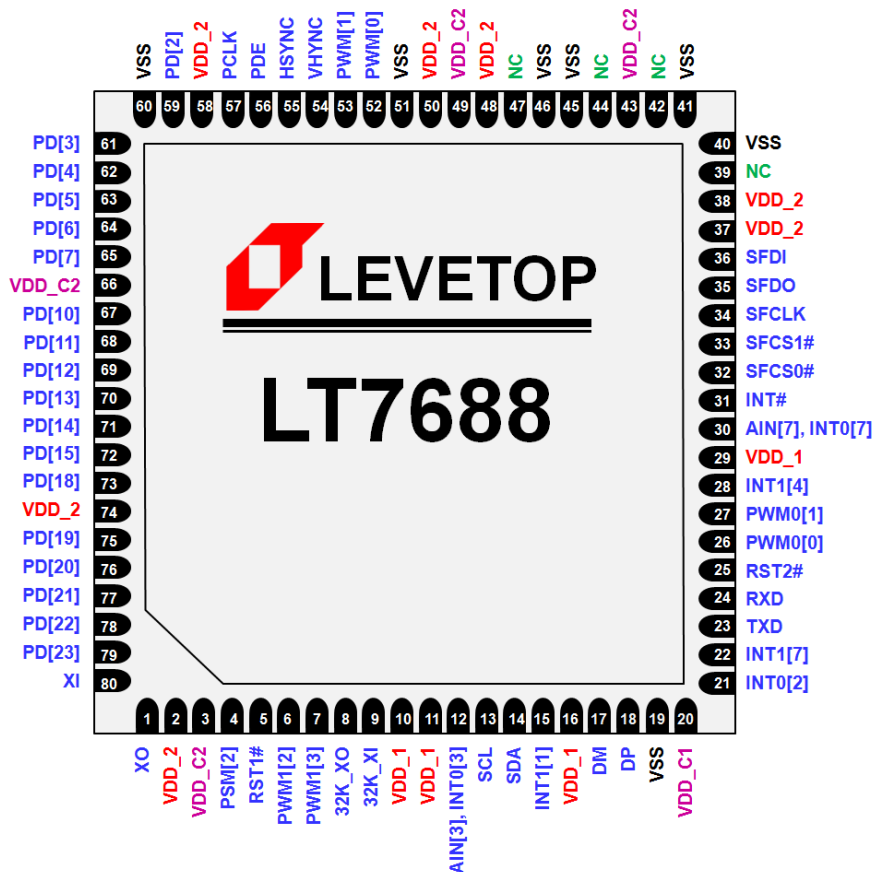- QFN-80Pin Package.

Temperature

- -40℃~85℃.

Pin Assignment

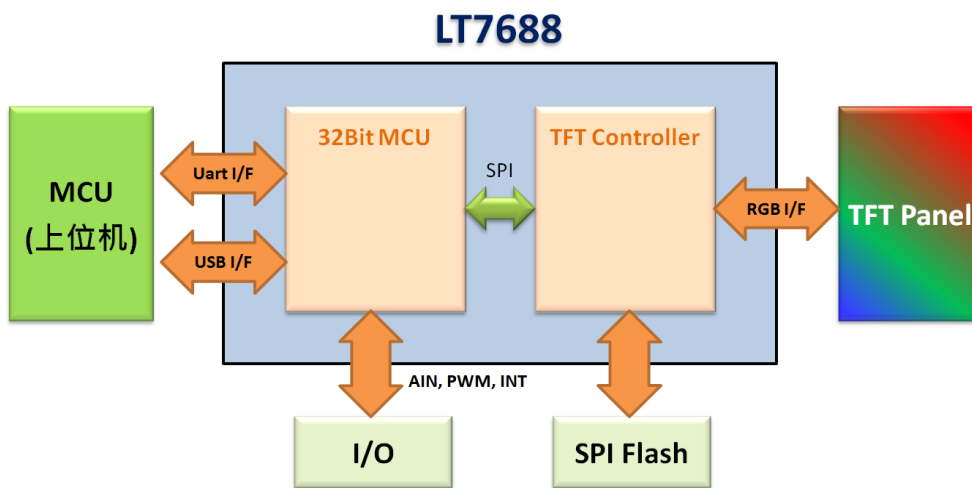**Figure 4: LT7688 Pin Assignment (QFN-80Pin)**

System Architecture

Figure 5: System Architecture Diagram

Pin Description

Uart Signals (2 Pins)

Table 2: Serial Uart Signals

Pin #	Pin Name	I/O	Pin Description
24	RXD		**SCI/Uart Receive Data** This is a Serial Communications Interface 0 Module Signal (SCI0). This signal is used for the SCI receiver data input and is also available for GPIO when not configured for receiver operation.
23	TXD		**SCI/Uart Transmit Data** This is a Serial Communications Interface 0 Module Signal (SCI0). This signal is used for the SCI transmitter data output and is also available for GPIO when not configured for transmitter operation.

USB Signals (2 Pins)

Table 3: USB Signals

Pin #	Pin Name	I/O	Pin Description
18	DP	IO	**USB Data Positive** These signals are used by the USB module.
17	DM	IO	**USB Data Negative** These signals are used by the USB module.

I2C Signals (2 Pins)

Table 4: I2C Signals

Pin #	Pin Name	I/O	Pin Description
13	SCL	IO	**I2C Clock** This signal is used for the I2C clock line signal and is also available for GPIO when not configured for receiver operation.
14	SDA	IO	**I2C Data** This signal is used for the I2C data line signal and is also available for GPIO when not configured for transmitter operation.

LCD Driver Signals (22 Pins)

Table 5: LCD Driver Signals

Pin #	Pin Name	I/O	Pin Description
79~75, 73, 72~67, 65~61, 59	PD[23:19], PD[18], PD[15:10], PD[7:3], PD[2]	IO	**LCD Panel Data Bus** TFT LCD data bus output for source driver. User can connect corresponding RGB bus for different setting. These are multiplex pins that share with GPIO pins. The Default setting of LCD interface is 18bpp function mode.
57	PCLK	O	**Panel Scan Clock** Generic TFT interface signal for panel scan clock. It derives from internal PLL.
54	VSYNC	O	**VSYNC Pulse** Generic TFT interface signal for vertical synchronous pulse.

Inner table (LCD Panel Data Bus):

Pin Name	TFT-LCD Interface	
	16bits	18bits
PD[2]	GPIOD[6]	B0
PD[3]	B0	B1
PD[4]	B1	B2
PD[5]	B2	B3
PD[6]	B3	B4
PD[7]	B4	B5
PD[10]	G0	G0
PD[11]	G1	G1
PD[12]	G2	G2
PD[13]	G3	G3
PD[14]	G4	G4
PD[15]	G5	G5
PD[18]	GPIOD[7]	R0
PD[19]	R0	R1
PD[20]	R1	R2
PD[21]	R2	R3
PD[22]	R3	R4
PD[23]	R4	R5

Table 5:**LCD Driver Signals (Continued)**

Pin #	Pin Name	I/O	Pin Description
55	HSYNC	O	**HSYNC Pulse** Generic TFT interface signal for horizontal synchronous pulse.
56	PDE	O	**Data Enable** Generic TFT interface signal for data valid or data enable.

External Serial Flash / SPI Master Signals (5 Pins)

Table 6:**External Serial Flash Signals**

Pin #	Pin Name	I/O	Pin Description
32	SFCS[0]# GPIOC[3]	IO	**Chip Select 0 for External Serial Flash or SPI device** SPI Chip select pin #0 for serial Flash or SPI device. If SPI master I/F is disabled then it can be programmed as GPIOC[3], and default is input function.
33	SFCS[1]# GPIOC[4]	IO	**Chip Select 1 for External Serial Flash or SPI device** SPI Chip select pin #1 for serial Flash or SPI device. If SPI master I/F is disabled then it can be programmed as GPIOC[4], and default is input function.
34	SFCLK GPIOC[0]	IO	**SPI Serial Clock** Serial clock output for serial Flash/ROM or SPI device. If SPI master I/F is disabled then it can be programmed as GPIOC[0], and default is input function.
35	SFDO GPIOC[1]	IO	**Master Output Slave Input** **Single Mode**: Data input of serial Flash or SPI device. For LT7688, it is output. **Dual Mode**: The signal is used as bi-direction data #0(SIO0). Only valid in serial flash DMA mode. If SPI master I/F is disabled then it can be programmed as GPIOC[1], and default is input function.
36	SFDI GPIOC[2]	IO	**Master Input Slave Output** **Single Mode**: Data output of serial Flash or SPI device. For LT7688, it is input. **Dual Mode**: The signal is used as bi-direction data #1(SIO1). Only valid in serial flash DMA mode. If SPI master I/F is disabled then it can be programmed as GPIOC[2], and default is input function.

PWM Signals (2 Pins)

Table 7：PWM Signals

Pin #	Pin Name	I/O	Pin Description
52	PWM[0] INITDIS GPIOC[7] CCLK	IO	**PWM Output #0 / Initial Display Enable** **PWM[0]**: PWM's output signal. The output mode is decided by configuration register. This pin can be used as the control signal of TFT panel's back light. **INITDIS**: Pull-high this pin will enable Initial Display function. This pin has internal pull-down in reset period to disable Initial Display function by default. i.e. after reset complete, internal pull-down resistor will be disabled. If PWM function disabled then it can be programmed as GPIO C[7], and default is GPIOC[7] input function, or output Core Clock - CCLK.
53	PWM[1]	IO	**PWM Output #1** PWM's output signal. The output mode and output function is decided by configuration register. This pin also can be used as the control signal of TFT panel's back light. When TEST[0] set high, then PWM[1] pin is external panel scan clock input
6, 7	PWM1[2], PWM1[3]	IO	**PWM1 Output Signals** These out signals function as either PMW1 output or GPIO.
26, 27	PWM0[0], PWM0[1]	IO	**PWM0 Output Signals** These out signals function as either PMW0 output or GPIO.

GPIO Signals (7 Pins)

Table 8：GPIO Signals

Pin #	Pin Name	I/O	Pin Description
52, 33, 32, 36, 35, 34	GPIOC[7] GPIOC[4:0]	IO	**GPIO C Group** These are general purpose I/O. GPIOC are available when PWM and SPI Master functions disabled. GPIOC[7] is same pin with PWM[0]. GPIOC[4:0] are multiplex pins that share with {SFCS1#, SFCS0#, SFDI, SFDO, SFCLK}
73, 59	GPIOD[7:6]	IO	**GPIO D Group** These are general purpose I/O. GPIOD[7] are multiplex pins that share with PD[18], and GPIOD[6] are multiplex pins that share with PD[2]. GPIOD[7,6] are available when LCD Panel interface is set 16bits.

Interrupt Signals (7 Pins)

Table 9: Interrupt Signals

Pin #	Pin Name	I/O	Pin Description
21, 12, 30	INT0[2], INT0[3], INT0[7]	IO	**Edge Port 0 Signals** These bidirectional signals function as either external interrupt sources or GPIO. INT0[3] is multiplex pin that share with AIN[3]. INT0[7] is multiplex pin that share with AIN[7].
15, 28, 22	INT1[1], INT1[4], INT1[7]	IO	**Edge Port 1 Signals** These bidirectional signals function as either external interrupt sources or GPIO.
31	INT#	O	**Interrupt Output Signal** The interrupt output for host to indicate the status of TFT controller.

Analog Input Signals (2 Pins)

Table 10: Analog Input

Pin #	Pin Name	I/O	Pin Description
12, 30	AIN[3], AIN[7]	IO	**ADC (Analog-to-Digital Converter) Input** These pins are analog input of ADC, and controlled by internal MCU register. AIN[3] is multiplex pin that share with INT0[3]. AIN[7] is multiplex pin that share with INT0[7].

Reset Signals (2 Pins)

Table 11: Reset Signals

Pin #	Pin Name	I/O	Pin Description
5	RST1#	I/O	**Reset Signal of TFT Controller** This is an active low Reset pin for TFT controller. To avoid noise interfere and cause fake reset behavior, this pin is active at least 256 OSC clocks.
25	RST2#	I/O	**Reset Signal of MCU** This active-low input signal is used as the external reset request. Reset places the CPU in supervisor mode with default settings for all register bits except some register bits only reset by POR. 0 = external reset assert 1 = external reset desert

Power and Clock Signals (25 pins)

Table 12: Power and Clock Signals

Pin #	Pin Name	I/O	Pin Description
80	XI	I	**Crystal / External Clock Input** This input pin is used for internal crystal circuit or external clock that generate clock source for PLL. It should be connected to external crystal or clock, and suggested frequency is 8 ~ 12MHz.
1	XO	O	**Crystal Output** This is an output pin for internal crystal circuit. It should be connected to external crystal circuit.
9	32K_XI		**32.768Khz Crystal Input** This pin is connect to 32.768Khz X'tal.
8	32K_XO		**32.768Khz Crystal Output** This pin is connect to 32.768Khz X'tal.
4	PSM[2]	I	Must tie to high level. (3.3V)
20	VDD_C1	PWR	**Internal LDO Output (1.2V)** These pins must connect 1uF and 0.1uF capacitor to ground.
3, 43, 49, 66	VDD_C2	PWR	**Internal LDO Output (1.8V)** These pins must connect 1uF and 0.1uF capacitor to ground.
10, 11, 16, 29	VDD_1	PWR	**3.3V Power Input**
2, 37, 38, 48, 50, 58, 74	VDD_2	PWR	**3.3V Power Input**
19, 40, 41, 45, 46, 51, 60,	VSS	PWR	**Ground Pins**
-	Thermal Pad	-	The back of LT7688 Heat Sink Pad must tie to ground.

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Function Description

The LT7688 combines high-performance 32bit MCU and TFT graphics accelerators. His internal MCU's main structure is the same as the Levetop's LT32U02, and its functions can be directly referenced to the LT32U02 specification and application manual. Therefore, the functional part of this specification for 32bit MCU will not be detailed. In addition, TFT Graphics Accelerator is the use of the Levetop's LT7680 hardware architecture, its connection to the MCU is shown in the following figure. This specification will be described as the specification of the TFT controller.
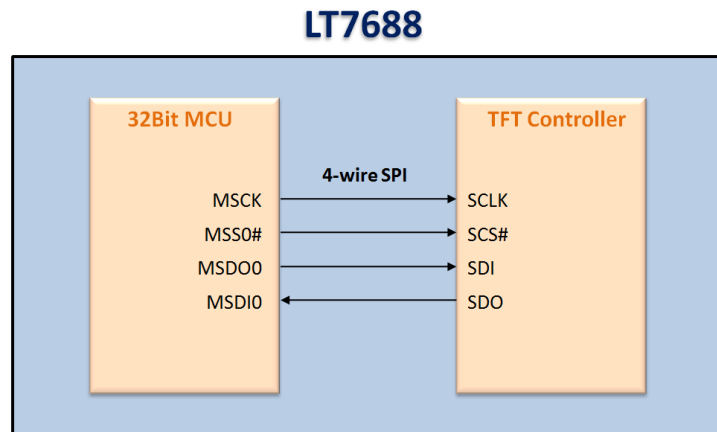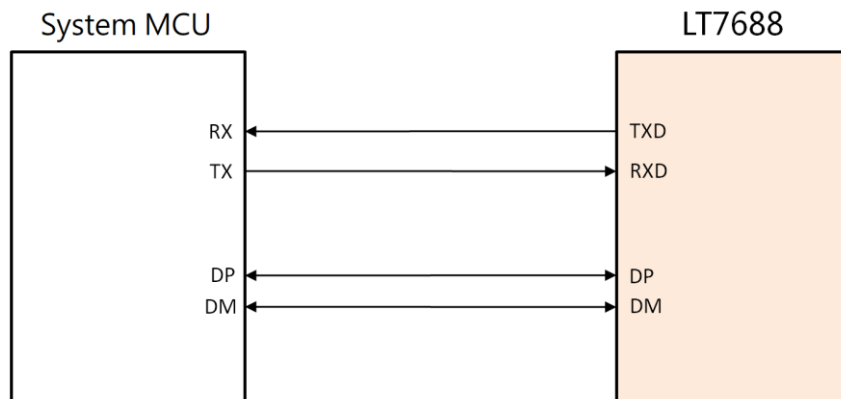

Figure 6: The connection of Internal MCU and TFT Controller

1. Communication Interface of System

The communication mode between LT7688 and System MCU is through the UART interface. Users can through the Levetop's development software for serial display development. The System MCU is responsible for sending display commands, while the LT7688 displays information such as pictures on the TFT Panel according to the display command. Levetop provides complete development and simulation environment. All display orders are planned and formulated by Levetop. For more information, please refer to our application manual.

In addition, System MCU can update LT7688 internal program or SPI Flash data via the USB interface.

Figure 7: The Connection of System MCU and LT7688

2. IO Interface

The LT7688's internal MCU module also offers many IO interfaces, as shown below in the left half. It includes 2 analog inputs, 6 interrupt signal inputs and 4 PWM signal outputs. These interfaces are set by the internal MCU registers and can also be used as normal GPIO. The Pin names are consistent with Levetop's LT32U02. The detailed operation can be found in the LT32U02 specification and application manual. And in the TFT controller also provides some GPIO interface, the right half of the image above. It can be used as an extension of the MCU interface. Usually these GPIO interfaces are shared with other control signals, as shown in Table 13 below. The GPIO pins can be used only when these control signals are prohibited.
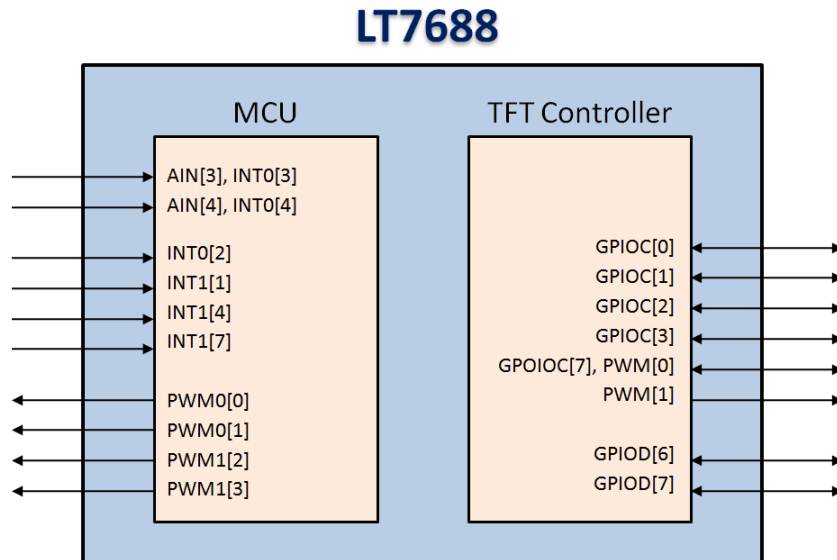

Figure 8: Internal I/O Interface

Table 13: The Alternate Pins of GPIO and Control Signals

| GPIO Pins	Alternate Signals
GPIOC[7]	PWM[0]
GPIOC[4:0],	{ SFCS1#, SFCS0#, SFDI, SFDO, SFCLK }
GPIOD[7:6],	{ PD[18], PD[2] }

The setting of these GPIO interfaces is determined by the Register REG F0h~F6h of the TFT Controller. Please refer to the Chapter 13 "Register Description" of the LT7680 specification.

3. Clock Signals

The clock signal architecture of LT7688 is shown in below Figure 9. The MCU section includes a 32KHz crystal oscillatory circuit with a separate power supply and two internal high-precision clock circuits (72MHz, 128KHz). The TFT controller consists of an external 10MHz crystal oscillation circuit and three internal PLL circuits. The clock signal of the TFT controller can be generated by a set of PWM outputs from the MCU (as show in Figure 9). Or use an external 10MHz crystal circuit (as shown in Figure 10).
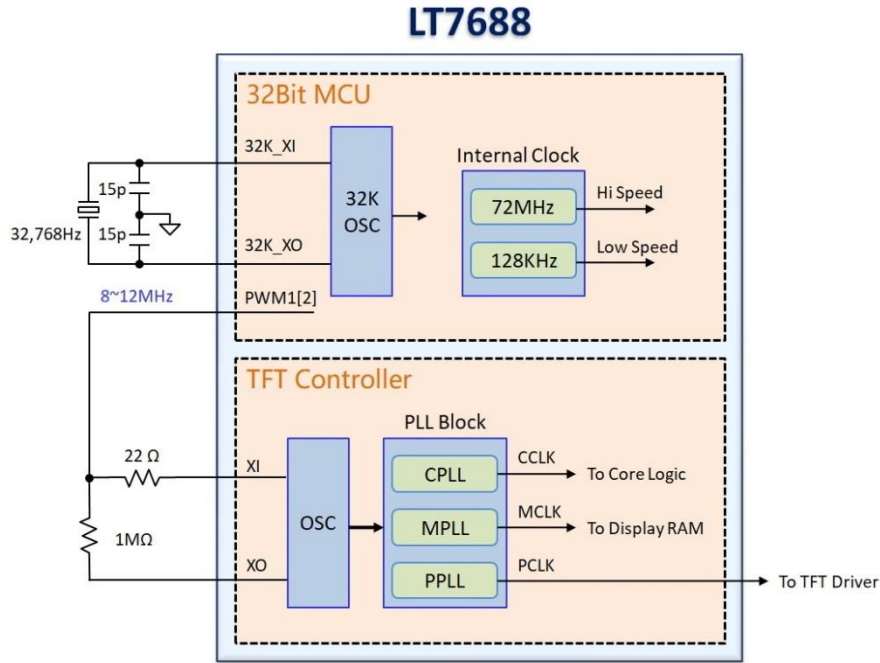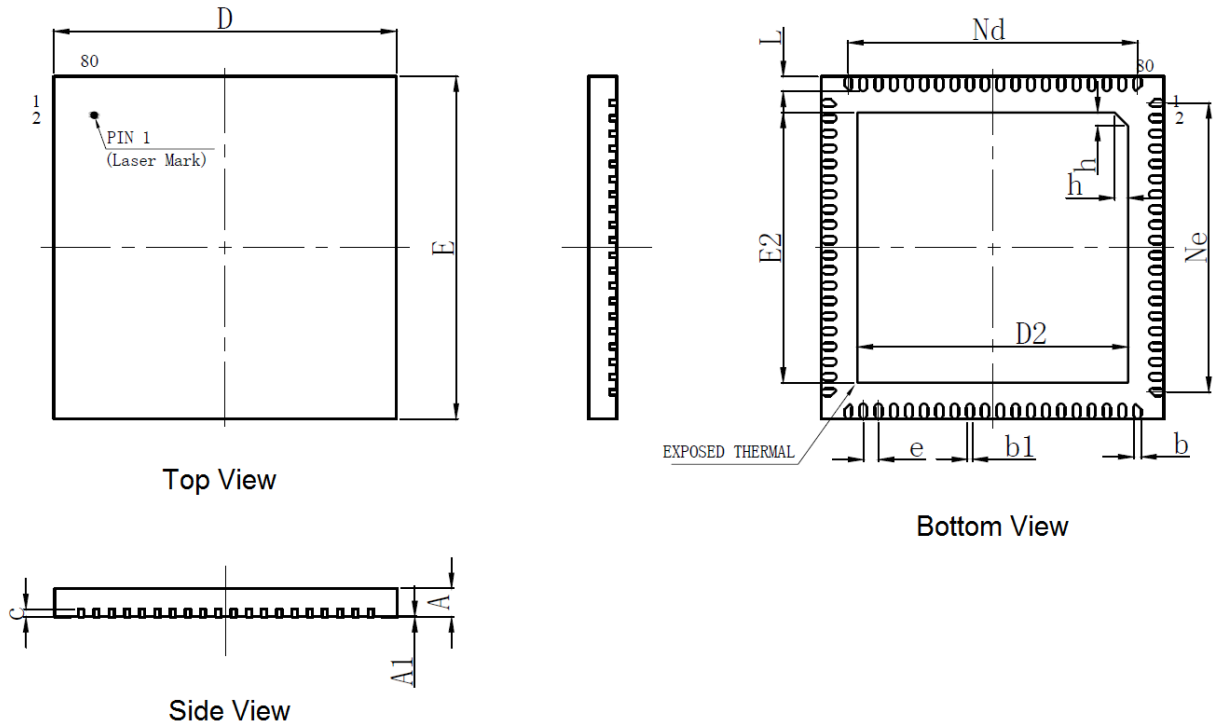
Figure 9: LT7688's Clock Structure
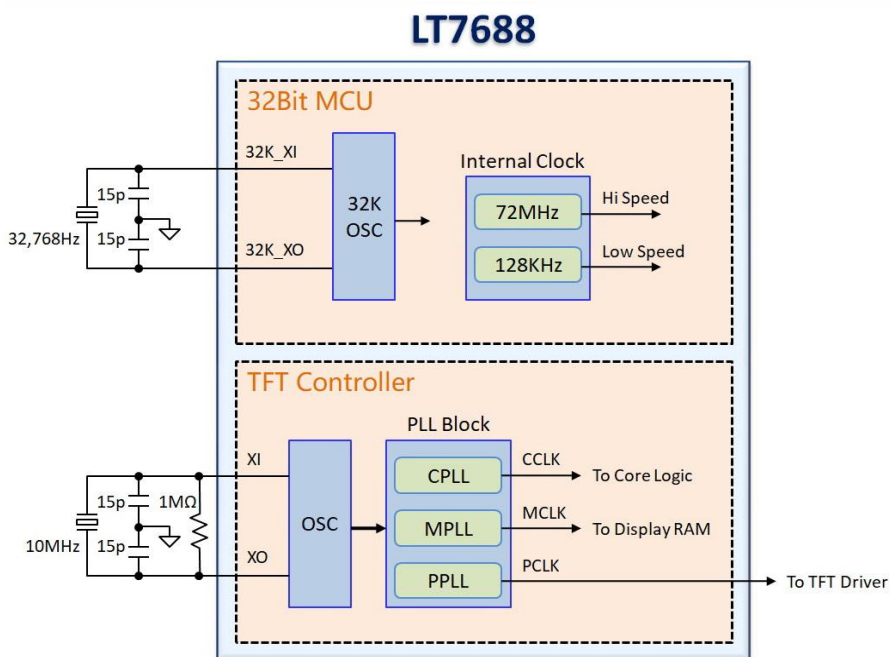
Figure 10: TFT Use External Xtal Oscillator

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Package Information

■ **LT7688 (QFN-80pin)**

Top View

Side View

Bottom View

Figure 11：**QFN-80Pin Outline**

Note: When PCB layout, the heat pad of LT7688's back (thermal Pad Zone) must be directly grounded.

Table 14：**QFN-80Pin Dimenstion**

Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max		Min.	Nom.	Max
A	0.70	0.75	0.8	**E**	8.9	9.0	9.10
A1	-	0.02	0.05	**Ne**		7.40BSC	
b	0.15	0.20	0.25	**L**	0.35	0.40	0.45
b1		0.14REF		**E2**	7.00	7.10	7.20
c	0.18	0.20	0.25	**h**	0.30	0.35	0.40
D	8.90	9.00	9.10	**Body Size**		295*295	
e		0.40BSC					
Nd		7.40BSC					